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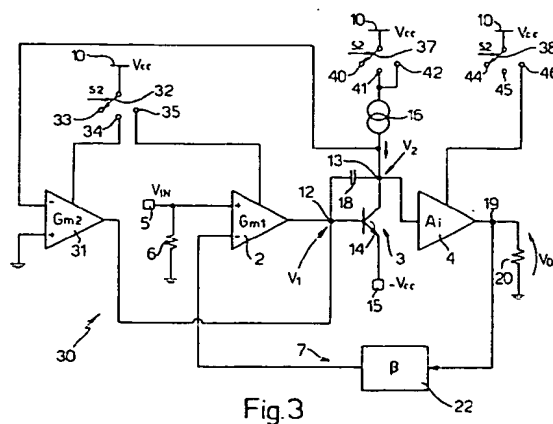
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Low frequency amplifier.

A low frequency amplifier (30) comprising, in series, a first input stage (2), an intermediate amplifying stage (3) and a final stage (4). The intermediate amplifying stage comprises a capacitor (18) which is discharged when the amplifier is disabled, and is charged to a predetermined bias value when the amplifier is operative. To prevent voltage peaks at the output of the amplifier (30) during the transient interval between the disabled and operating condition of the amplifier, a second input stage (31) is provided which is only turned on during the transient interval, and is connected to the capacitor (18) to detect its voltage and charge it. During the transient interval, the final stage (4) is disabled. Upon the capacitor (18) reaching the predetermined charge value, the second input stage practically turns itself off, and is then disabled; and, at the same time, the first input stage (2) and the final stage (4) are enabled to turn on the amplifier (30).



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The present invention relates to a low frequency amplifier, in particular a high quality audio amplifier with split supply which is symmetrical with respect to ground, the load connected directly between the amplifier output and ground, and no decoupling capacitor.

As is known, at present, amplifiers of the above type present a standby function wherein the amplifier is supplied but the current paths are interrupted as far as possible to minimize (theoretically eliminate) absorption; in that condition, any signals at the input are not transferred to the output of the amplifier.

For clearness, a typical audio amplifier of the above type will be described with reference to the block diagram in Figure 1.

The Figure 1 amplifier, indicated as a whole by 1, is substantially composed of three cascade stages: an input stage 2; a voltage amplifying stage 3; and an output stage 4 operating as a current amplifier.

Input stage 2 comprises a transconductance amplifier (also indicated Gm1), i.e. an amplifier with a voltage input and a current output, and presents a noninverting input connected to an input terminal 5 supplied with an input signal V_{IN} to be amplified. An input resistor 6 is also provided between terminal 5 and ground. Input stage 2 also presents an inverting input connected to a feedback line 7, and is connected to a first supply line 10 (at voltage V_{CC}) via a first switch 11 controlled by a logic signal S1.

Voltage amplifying stage 3 is exemplified by a transistor 14, here a bipolar NPN type, with the base terminal connected to the output of input stage 2 (node 12), the emitter terminal connected to a second supply line (terminal 15) at voltage $-V_{CC}$, and the collector terminal (node 13) connected to a current source 16 which is also connected to first supply line 10 via a second switch 17 also controlled by signal S1. A compensating capacitor 18 is provided between the collector and base terminals of transistor 14.

Output stage 4 substantially operates as a buffer, and presents an input connected to the collector terminal of transistor 14, and an output 19 defining the output of amplifier 1 and connected directly to one terminal of a load 20, represented here by a resistor which is grounded at the other terminal. The voltage across load 20 is indicated V_O . Output stage 4 is connected to first supply line 10 via a third switch 21 controlled by the same logic signal S1 as switches 11, 17, so that, when switch 21 is open, output stage 4 is turned off and disconnects the load from the rest of amplifier 1.

Feedback line 7 comprises a block 22 having a transfer function β and connected between output 19 of amplifier 1 and the inverting input of input

stage 2.

When the Figure 1 amplifier is in standby mode, logic signal S1 assumes a level (indicated 0 in Figure 2) corresponding to the open condition of switches 11, 17 and 21, so that stages 2, 3 and 4 are disconnected from the positive supply; voltage V_1 with respect to ground at the base terminal and voltage V_2 at the collector terminal of transistor 14 are equal $V_1 = V_2 = -V_{CC}$, i.e. equal the negative supply voltage of line 15; capacitor 18 is discharged; and output voltage V_O is zero (Figure 2).

When amplifier 1 is turned on, logic signal S1 switches to a logic stage ("1" in Figure 2) such as to close switches 11, 17, 21, so that stages 2-4 are turned on, and amplifier 1 evolves towards the balanced bias condition (steady state). More specifically, in the transient interval, capacitor 18 is charged from 0 V to V_{CC} so that voltage V_2 is brought from $-V_{CC}$ to 0 V; and voltage V_O at the load follows voltage V_2 at the input of the final stage, so that, when switch 21 is closed and final stage 4 turned on, it presents a negative peak followed by an increase up to the steady-state value, as shown in Figure 2.

To eliminate the negative peak, nodes 12 and 13 may be appropriately biased by connecting them to voltage sources of a predetermined value and which are only active in the transient interval from standby mode. Such a solution, however, is difficult to implement in that, for it to function properly, the value of the voltages supplied depends on the specific circuit involved and is highly unpredictable (especially as regards voltage V_1 at node 12).

Neither is it possible to simply keep final stage 4 off during the transient interval, as this would not guarantee circuit 1 reaching the steady-state condition. If such were the case, in fact, input stage 2 would be unaware of developments in the circuit via feedback branch 7 by virtue of node 13 being disconnected from node 19 to which input stage 2 is connected.

It is an object of the present invention to provide a low frequency amplifier designed, by means of a simple, widely applicable solution, to overcome the problem of the negative peak in the output voltage.

According to the present invention, there is provided a low frequency amplifier as claimed in Claim 1.

A preferred, non-limiting embodiment of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows a block diagram of a typical amplifier of the type considered;

Figure 2 shows a diagram of a number of signals relative to the Figure 1 amplifier;

Figure 3 shows a block diagram of the amplifier according to the present invention;

Figure 4 shows a diagram of a number of signals relative to the Figure 3 amplifier;

Figure 5 shows an example embodiment of the circuitry of the amplifier according to the present invention.

Number 30 in Figure 3 indicates a low frequency amplifier presenting the same basic structure as amplifier 1 in Figure 1, so that any parts common to both are indicated using the same numbering system with no detailed description.

As shown in Figure 3, circuit 30 comprises a second input stage 31 (transient input stage) also formed by a transconductance amplifier (Gm2), and presenting a grounded noninverting input, an inverting input connected to node 13, and the output connected to node 12. Input stages 2 and 31 are connected to V_{CC} supply line 10 via a three-position switch 32 controlled by a signal S2. More specifically, in a first position (shown in Figure 3), switch 32 connects supply line 10 to a node 33 not connected to any point; in a second position, it connects supply line 10 to a node 34 connected to second input stage 31; and in a third position, it connects line 10 to a node 35 connected to first input stage 2.

Similarly, voltage amplifying stage 3 and output stage 4 are connected to supply line 10 via respective three-position switches 37, 38 also controlled by signal S2. More specifically, switch 37 is movable between a first position (shown in Figure 3) wherein it connects supply line 10 to a no-load node 40, and a second and third position wherein it connects supply line 10 to nodes 41, 42, both connected to node 13 via current source 16. Switch 38 is movable between a first and second position wherein it connects supply line 10 to disconnected nodes 44, 45, and a third position wherein it connects line 10 to a node 46 connected to output stage 4.

Operation of the Figure 3 circuit will now be described with reference also to the signal diagram in Figure 4. In the signal S2 plot, 0, 1 and 2 respectively indicate a first, second and third value of signal S2, corresponding respectively to the first, second and third position of switches 32, 37, 38.

In standby mode, signal S2 presents a 0 value corresponding to the first position of switches 32, 37, 38, i.e. the position shown in Figure 3, in which case, none of stages 2-4 is supplied; voltage V_0 at the load is zero (0 V); and voltages V_1 , V_2 at nodes 12, 13 are at $-V_{CC}$.

At instant t_1 , signal S2 switches to 1 corresponding to the second position of switches 32, 37, 38. Consequently, switch 32 connects supply line 10 to node 34, so that second input stage 31 is supplied, and first input stage 2 remains off; switch

37 connects line 10 to node 41, so that voltage amplifying stage 3 is supplied; and switch 38 connects line 10 to node 45, so that output stage 4 remains unsupplied.

At this phase, therefore, output stage 4 continues operating like an open switch, and node 13 remains disconnected from output node 19; whereas second input stage 31 is turned on, and compares the voltages at its inputs. More specifically, and in known manner, stage 31 drives node 12 so as to reduce the unbalance between its inverting input (connected to node 13) and its (grounded) noninverting input; for which purpose, it draws current from the supply via source 16 and capacitor 18, which current charges capacitor 18, thus increasing voltage V_2 at node 13. This continues until voltage V_2 reaches 0 V (balanced condition of the inputs of stage 31) as shown in Figure 4, after which, second input stage 31 practically turns itself off, leaving the circuit in the balanced condition achieved.

At instant t_2 , signal S2 again switches, this time to value 2, so that switches 32, 37, 38 are set to the third position wherein switch 32 connects supply line 10 to node 35, thus cutting off supply to second input stage 31 and supplying first input stage 2; switch 37 connects line 10 to node 42 so that voltage amplifying stage 3 remains supplied; and switch 38 connects line 10 to node 46, thus supplying output stage 4. As such, circuit 30 is now operative with stages 2-4 supplied and stage 31 disabled.

In other words, in the transient interval, the final stage is turned off to prevent the signal transients from reaching the output, and, at the same time, input stage 2 is replaced by a stage (amplifier 31) for bringing the circuit into the balanced condition by charging compensating capacitor 18 to the required value, so that no negative pulses occur at the output, and the circuit is brought automatically into the steady-state condition. Conversely, in steady-state mode, second input stage 31 is turned off, and circuit 30 corresponds exactly, in terms of structure and operation, to the known circuit in Figure 1.

Figure 5 shows one possible circuit arrangement for implementing input stages 2, 31 as shown in Figure 3.

More specifically, in the Figure 5 arrangement, stages 2, 31 each present a respective differential circuit 50, 51, and a common single-output load circuit 52. Differential circuits 50 and 51 are of known type, and each comprise a first transistor 54, 55, and a second transistor 56, 57, all PNP types. The emitter terminals of transistors 54, 56 are connected to each other via respective resistors 58, 59 and to node 35; the emitter terminals of transistors 55, 57 are connected to each other via

respective resistors 60, 61 and to node 34; the base terminals of transistors 54, 56 define the inputs of differential circuit 50, and are therefore connected respectively to input node 5 and feedback block 22; the base terminals of transistors 55, 57 define the inputs of differential circuit 51, and are respectively grounded and connected to node 13; the collector terminals of transistors 54, 55 are connected to the collector terminal of a transistor 64 forming part of common load circuit 52; and the collector terminals of transistors 56, 57 are connected to the collector terminal of a transistor 65 also forming part of common load circuit 52.

Load transistors 64, 65 are NPN types, with the base terminals connected to each other, and the emitter terminals both connected to node 15 supplying negative supply voltage $-V_{CC}$. Transistor 65 is diode-connected; and the collector terminal of transistor 64 defines the output of load circuit 52, which is connected to node 12.

Figure 5 also shows a current source 66 for biasing input stages 2, 31.

The Figure 5 circuit operates in the same way as described for circuit 30 in Figure 3.

The Figure 5 circuit presents the advantage of compactness by virtue of stages 2 and 31 sharing load circuit 52 and bias source 66. What is more, the circuit provides for a high degree of reliability by virtue of second input stage 31 being turned off in steady-state mode, and by virtue of requiring no alteration of stages 2-4 with respect to known amplifiers.

Clearly, changes may be made to the amplifier as described and illustrated herein without, however, departing from the scope of the present invention. In particular, the same inventive idea may also be applied to amplifiers featuring a voltage amplifying stage in the form of a MOS transistor requiring charging of the gate capacitance in the turn-on transient interval without producing a voltage peak at the output. Also, switches 32, 37, 38 may be formed in any appropriate manner, each by means of one or more switching elements appropriately controlled by one or more, e.g. digital, signals.

Claims

1. A low frequency amplifier (30) comprising, in series, an input stage (2), an intermediate amplifying stage (3) and a final stage (4), wherein said intermediate amplifying stage comprises a capacitive element (18) chargeable between a first value when said amplifier is disabled, and a second value when said amplifier is operative; characterized in that it comprises switchable source means (31) connected to said capacitive element (18), for supplying said

capacitive element with a charge signal; enabling means (32) for enabling said source means during the transient interval from said disabled condition to said operating condition of said amplifier; and disabling means (38) for disabling said final stage (4) during said transient interval.

2. An amplifier as claimed in Claim 1, characterized in that said source means comprise voltage detecting means (31) connected to said capacitive element (18), for disabling said source means upon said second charge value of said capacitive element being reached.
3. An amplifier as claimed in Claim 1 or 2, characterized in that said enabling means comprise a first switch element (32); said first switch element being connected to a first reference potential line (10), to said input stage (2), and to said source means (31), and selectively connecting said input stage or said source means to said first reference potential line.
4. An amplifier as claimed in one of the foregoing claims from 1 to 3, wherein said input stage comprises a first transconductance amplifying stage (2); characterized in that said source means comprise a second transconductance amplifier (31).
5. An amplifier as claimed in Claim 4, wherein said capacitive element (18) presents a first terminal connected to the input node (13) of said final stage (4), and a second terminal connected to the output node (12) of said input stage (2); characterized in that said second transconductance amplifier (31) comprises a first input connected to said first terminal (13) of said capacitive element (18); a second input connected to a second reference potential line; and an output connected to said second terminal (12) of said capacitive element.
6. An amplifier as claimed in Claim 5, of the split supply type, comprising a first (10), a second and a third (15) reference potential line; said second reference potential line defining a ground line; and said first (10) and third (15) reference potential lines presenting a potential of the same value and opposite sign with respect to said ground line; characterized in that said second input of said second transconductance amplifier (31) is connected to said ground line.
7. An amplifier as claimed in one of the foregoing Claims from 4 to 6, characterized in that said

first and second transconductance stages (2, 31) each comprise a respective differential circuit (50, 51); a common single-output load circuit (52); and a common bias source element (66).

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8. An amplifier as claimed in one of the foregoing claims from 1 to 7, characterized in that said disabling means comprise a second switch element (38) connected between a first reference potential line (10) and said final stage (4), and connecting said final stage to said first reference potential line at the end of said transient interval.

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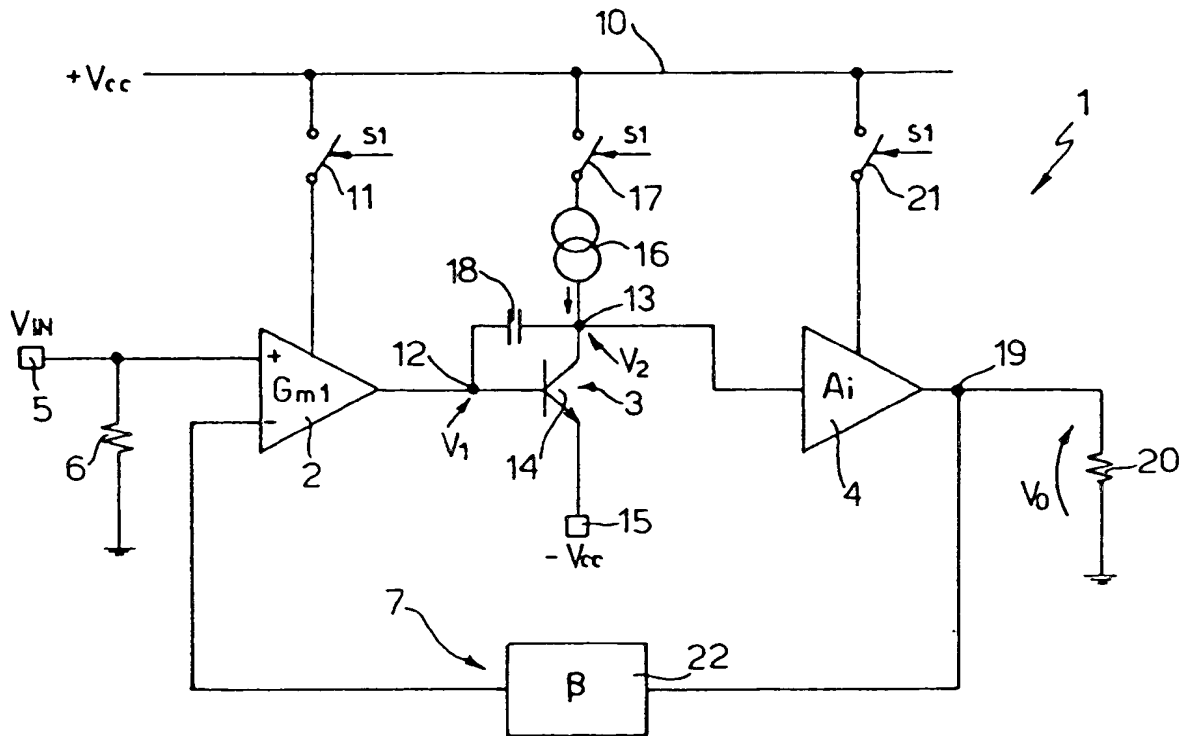


Fig.1

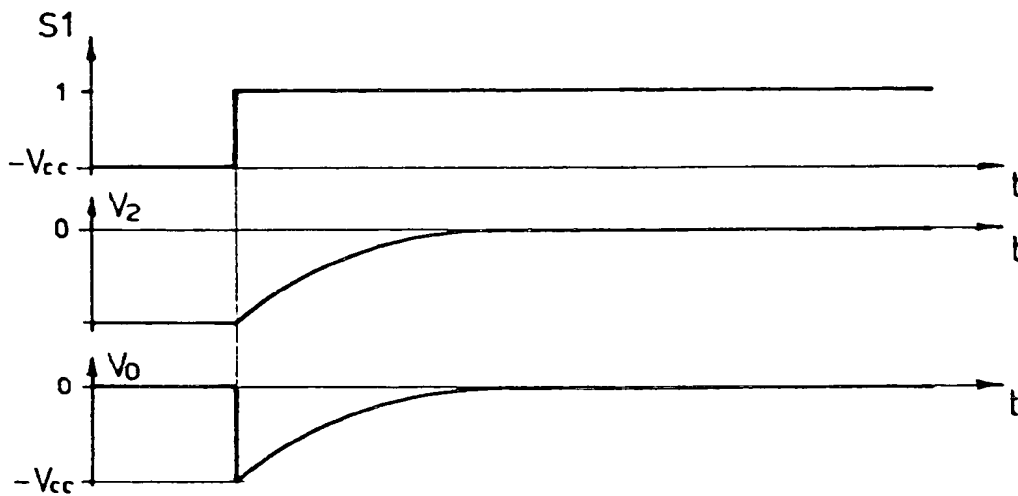


Fig.2

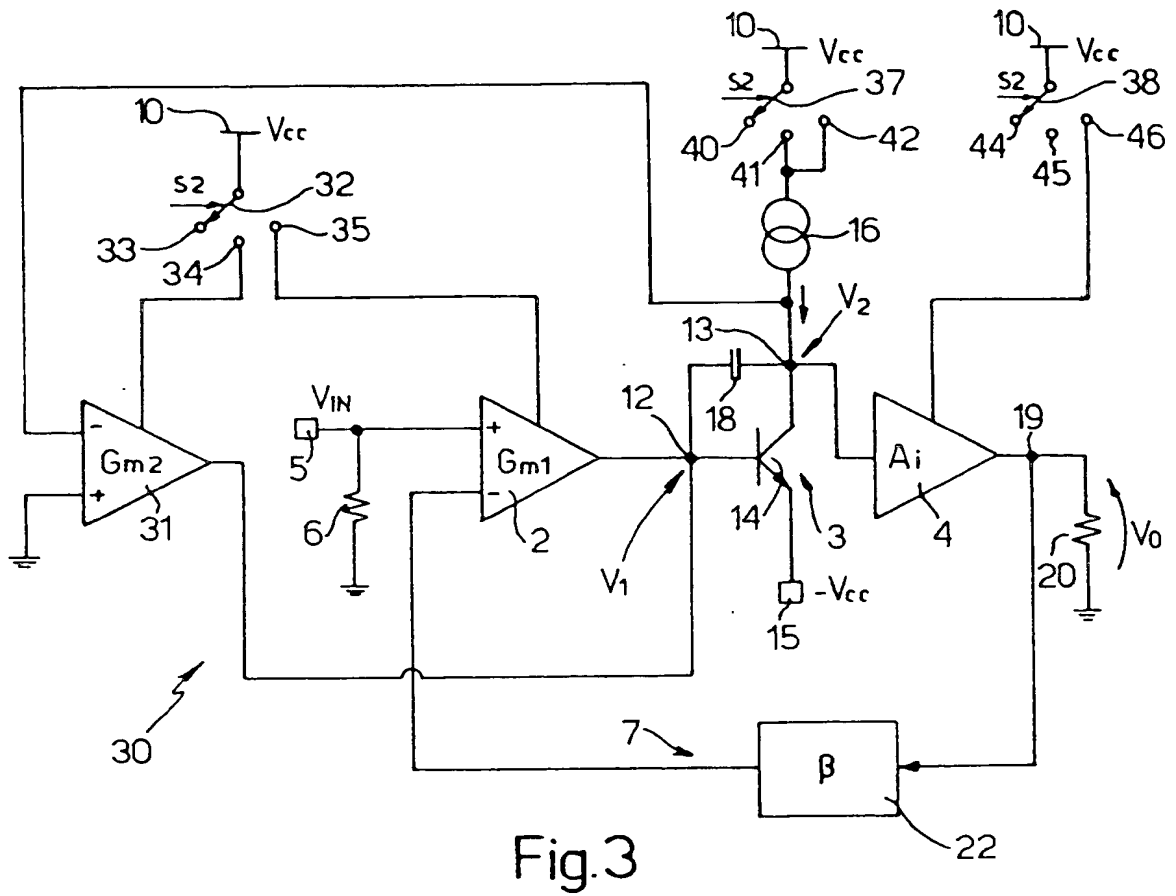


Fig. 3

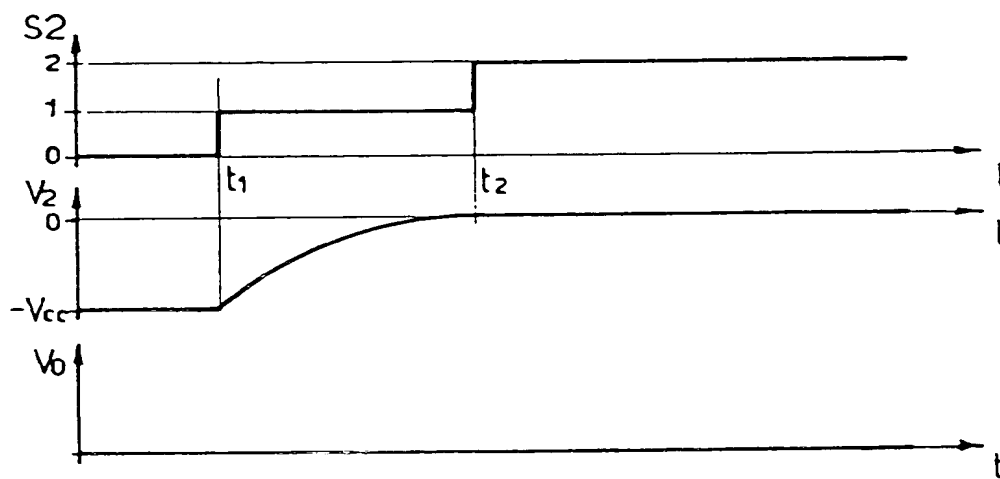
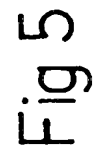


Fig. 4





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EUROPEAN SEARCH REPORT

Application Number
EP 94 83 0179

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	PATENT ABSTRACTS OF JAPAN vol. 17, no. 283 (E-1373) 31 May 1993 & JP-A-05 014 061 (SUZUKI TAKEFUMI) * abstract *	1	H03F1/30 H03G3/34
A	EP-A-0 185 411 (PHILIPS' GLOEILAMPENFABRIEKEN) * page 5, line 16 - page 6, line 28; figures 1,2 *	1	
A	US-A-5 166 983 (D. M. SUSAK) * column 3, line 1 - column 4, line 62; figure 2 *	1	
A	EP-A-0 299 665 (KABUSHIKI KAISHA TOSHIBA) * abstract *	1	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H03F H03G
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 15 September 1994	Examiner Blaas, D-L
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